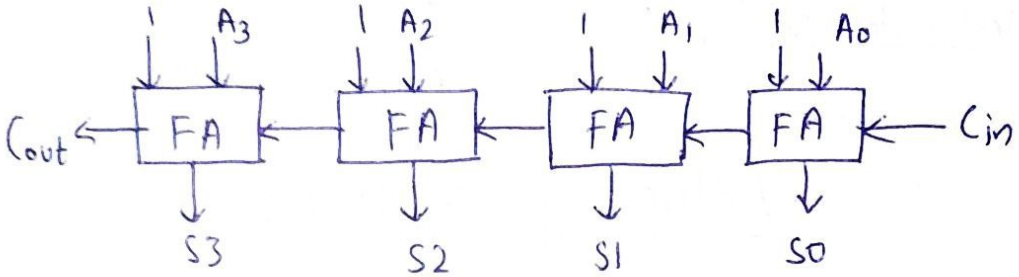
Section - D

Q-① (a) It subtracts 1 binary value from existing binary value stored in the register. It decreases the existing value stored in the register by 1.

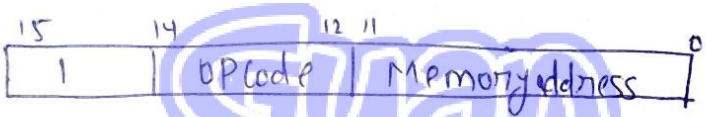
In case of 4 bit binary decrementer we require 4 Full adders.



4-Bit Binary decrementer

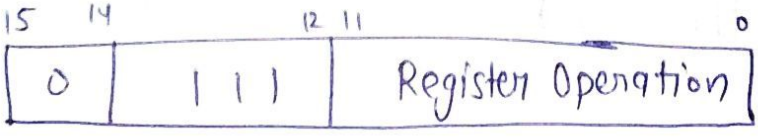
(b) Basic computer has 16 bit instruction register (IR) which can denote either memory reference or I/O.

(i) Memory Reference :- It refers to memory address an an operand.



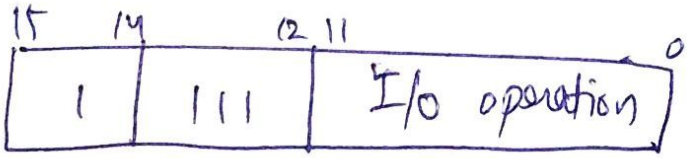
(ii) Register Reference :- It performs operations on register rather than memory address

The IR(14-12) is 111 & IR(15) is 0

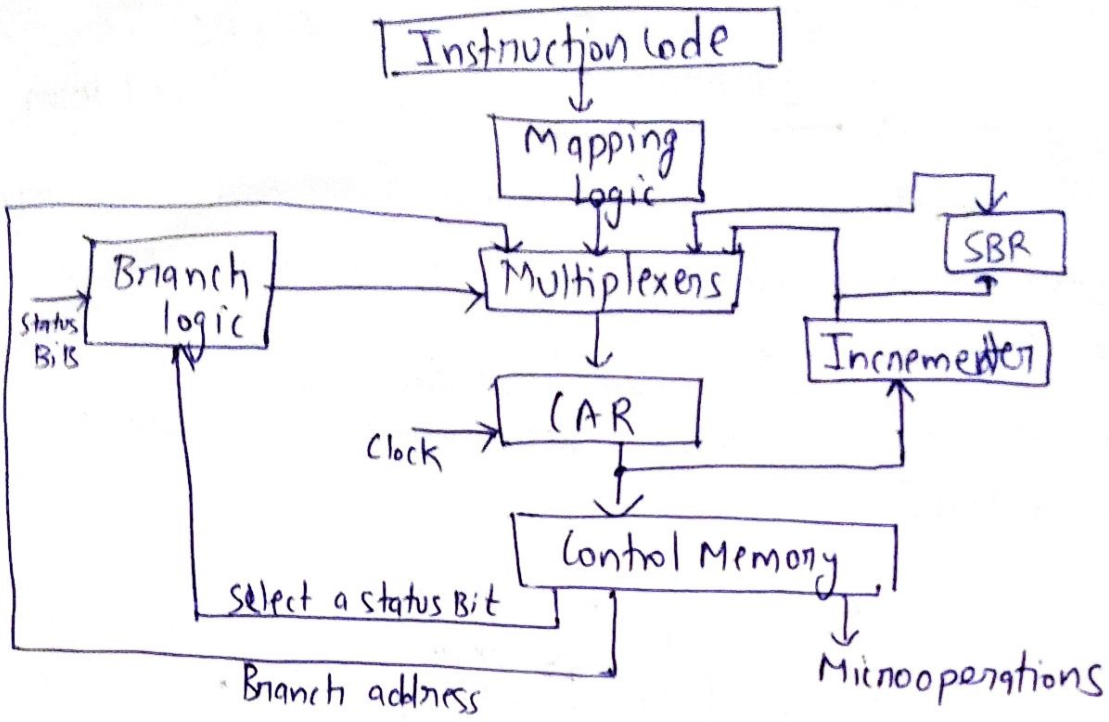


(iii) I/O :- It is comm^n b/w computer & outside environment

IR(14-12) is 111 & IR(15) = 1



Er Sahil Ka Gyan



Addressing Sequencing

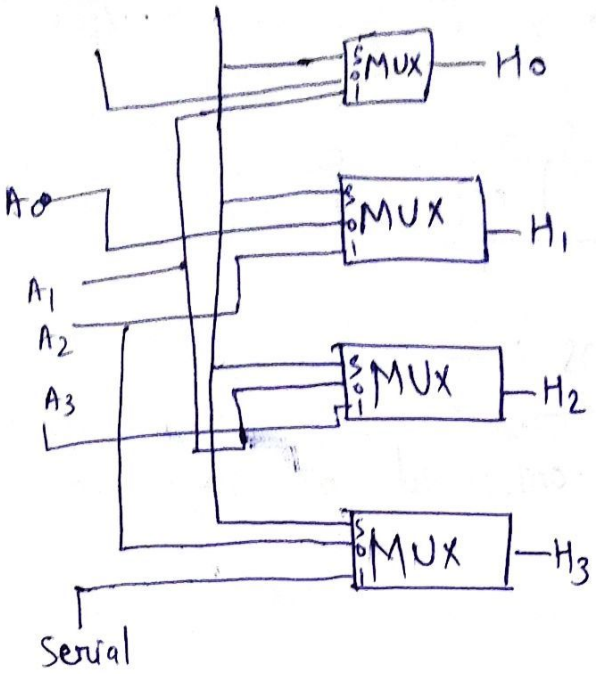
(c) Shift micro operations => It is used for serial transfer of information. These are also used in conjunction with arithmetic, logic micro operations.

Types of SMO:-

(i) Logical:- It transfers the zero through the serial input. We use the symbols for logical shift left & right.

(ii) Arithmetic :- It shifts a signed binary number to the left or to the right position.

(iii) Circular :- This shift circulates the bits in the sequence of register around the both ends without any loss of information.



Function table

S	H_0	H_1	H_2	H_3
0	I_R	A_0	A_1	A_2
1	A_1	A_2	A_3	I_L

Section (B)

Q.2 **Register Transfer Language:-** It is the symbolic representation of the notations used to specify the sequence of micro operations.

→ Information transfer from one register to another is called Register Transfer.

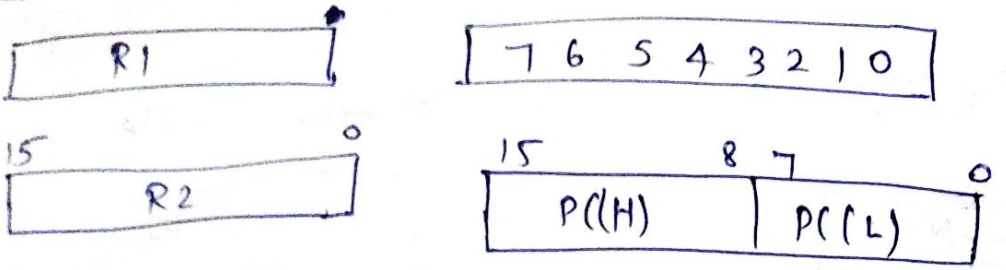
→ Registers are designated by capital letters, sometimes followed by numbers. (Eg- A, R1, R13, IR)

Symbol	Description	Example
Capital letters	Denotes register	MAR, R2
( )	Denotes a part of a register	R(0-7), R2(4)
←	Denotes transfer of info.	R2 ← R1
:	Denotes termination	
;	Separates 2 micro-operations	A ← B, B ← A

MAR → memory address register

PC → Program counter

IR → Instruction Register.



Arithematic Micro Operations :—

This Micro operations are performed on numeric data stored in registers.

It may includes :—

Addition, subtraction, complement, increment, decrement

Symbolic Designation	Description
$R_3 \leftarrow R_1 + R_2$	R_1 plus R_2 transfer into R_3
$R_3 \leftarrow R_1 - R_2$	R_1 minus R_2 transfer into R_3
$R_2 \leftarrow \overline{R_2}$	Complement of R_2
$R_2 \leftarrow \overline{R_2} + 1$	2's complement
$R_3 \leftarrow R_2 + \overline{R_2} + 1$	R_1 + 2's complement of R_2
$R_1 \leftarrow R_1 + 1$	Increagment by 1
$R_1 \leftarrow R_1 - 1$	Decrement by 1

Ay-(3)

Introduction of Assembler :—

Assembler is a program for converting instructions written in low-level assembly code into relocatable machine code & generating along information for the loader.

If assembler do all this work in one scan then it is called multiple pass assembler.
Here assembler divide these tasks in 2 passes

Pass 1 :-
Define symbols & literals and remember them in symbol table & literal table respectively.
keep track of location counter.
Process pseudo-operation

Pass 2 :- Generate object code by converting symbolic op-code into respective numeric op-code.
Generate data for literals and look for values of symbols

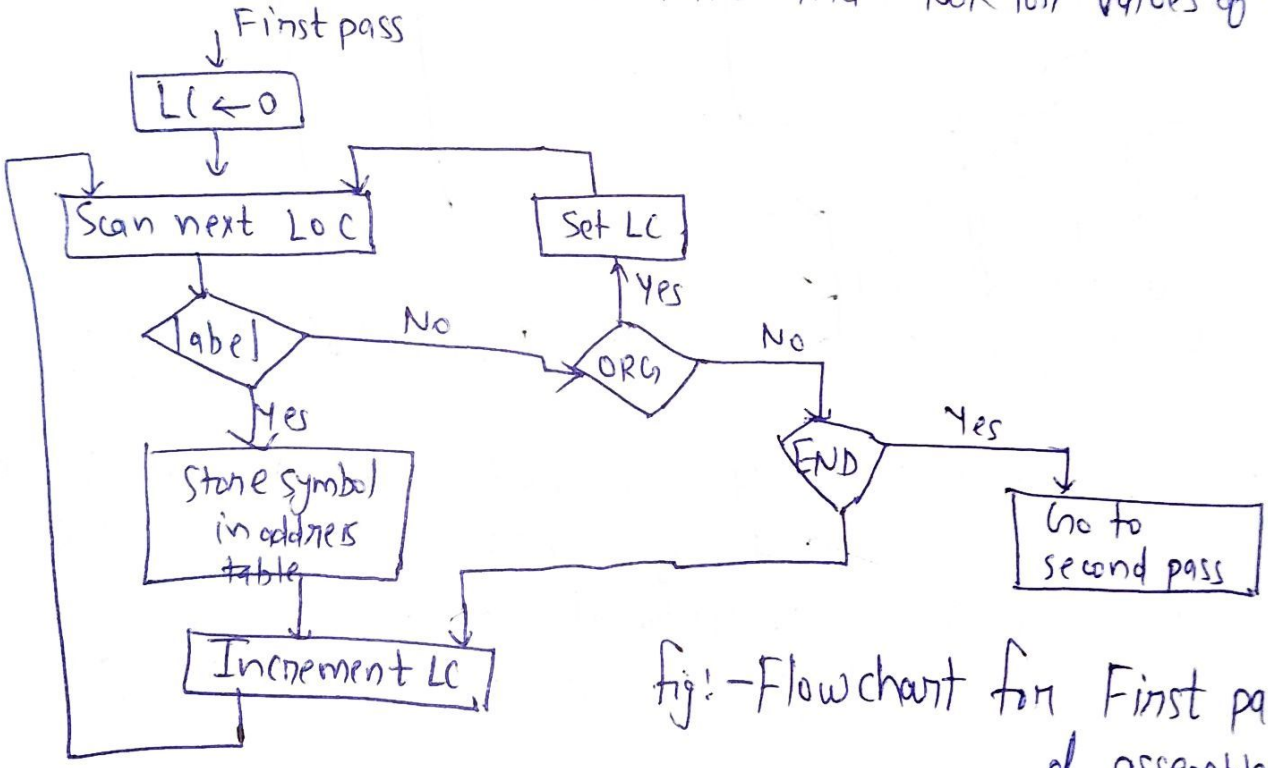


fig:-Flowchart for First pass of assembler

Er Sahil Ka Gyan

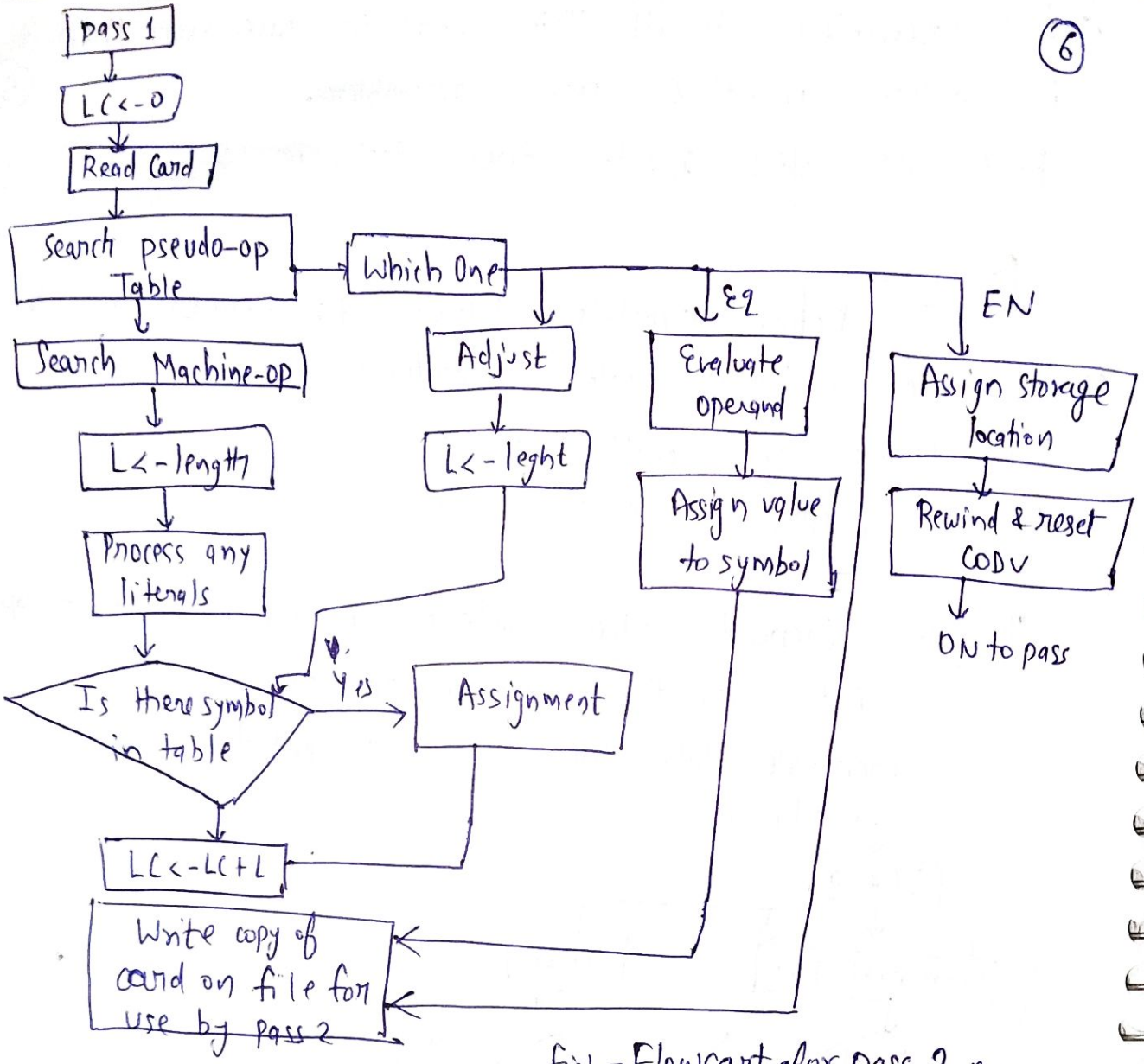
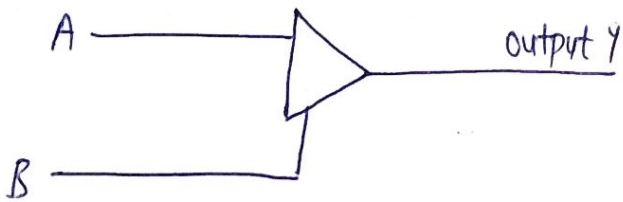


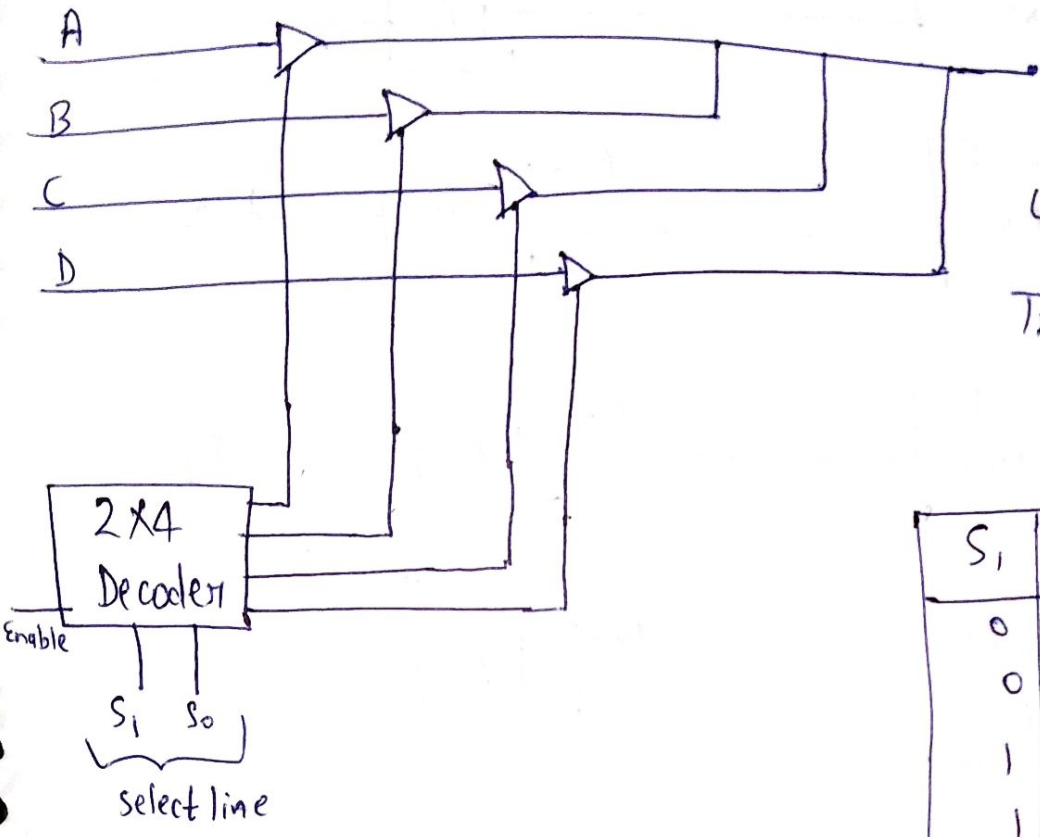
fig:- Flowcart for pass 2

Ans (4) Tri state Buffer:- It is a digit circuit that has 3 gates two of which are signals equivalent to logic 1&0 as in a conventional gate.
However, the third gate exhibits a high-impedence gate.



Y = A if C = 1
High Impedence if C = 0

Bus line with 3 state Buffer:-



one line common Bus system using Tri-state Buffer

S_1	S_0	Y
0	0	A
0	1	B
1	0	C
1	1	D

In tri-state, logic allows an output or input to assume a high impedence state, effectively removing the o/p from the circuit, in addition to the 0 & 1 logic levels.

Ay (5)

8 bit **ALU** was formed by combining three 4 bit ALU's with 5 multiplexers. The 8 bit ALU is based on use of carry select line. The Four lowest bits are fed into one of the 4 bit ALU's.

The O/p of selectable ALU's are multiplexed together forming the upper & lower 4 bits & carry out for 8 bit ALU.

SAHIL KHAN

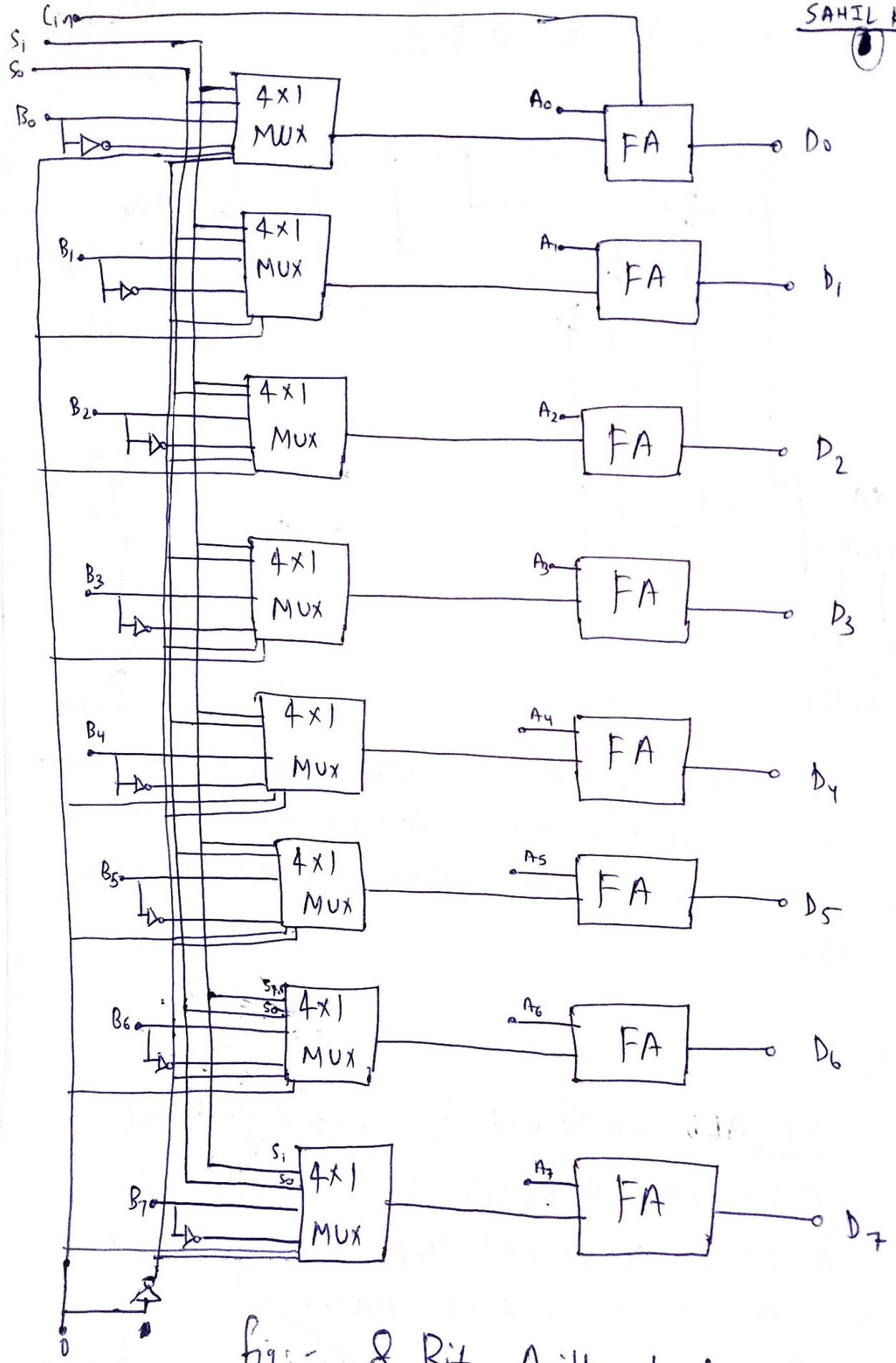


fig:- 8 Bit Arithmetic Circuit

Ans 1 **Virtual Memory :-** In a memory hierarchy system, programs & data are first stored in auxiliary memory.

→ Portions of a program or data are brought into main memory as they are needed by the CPU.

→ VM is a concept based in some large computer systems that permit the user to construct programs as though a large memory space were available, equal to the totality of auxiliary memory.

→ Each address that is referenced by CPU goes through an address mapping from the so-called virtual address to physical address in main memory.

Address space & Memory Space →

An address used by a programmer will be called a virtual address and the set of such addresses the address space. An address in main memory is called a location or physical address. The set of such locations is called the memory space.

→ The address space is allowed to be larger than memory space in computers with virtual Memory.

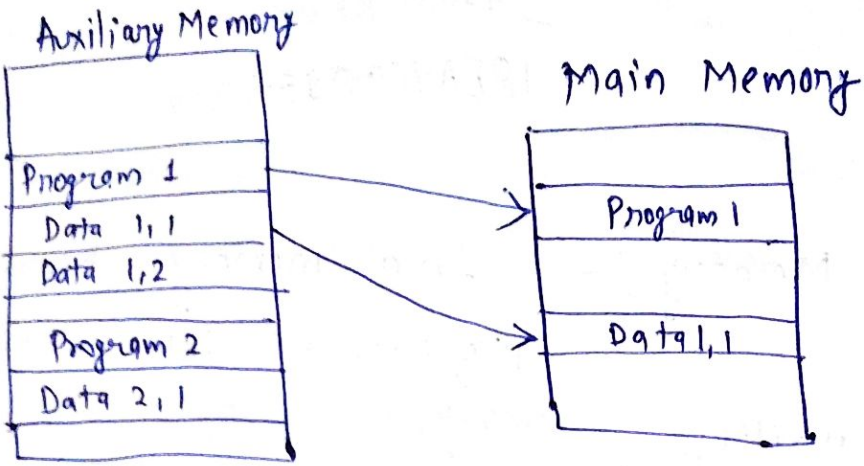


fig:- Relation B/w address & memory space in VM

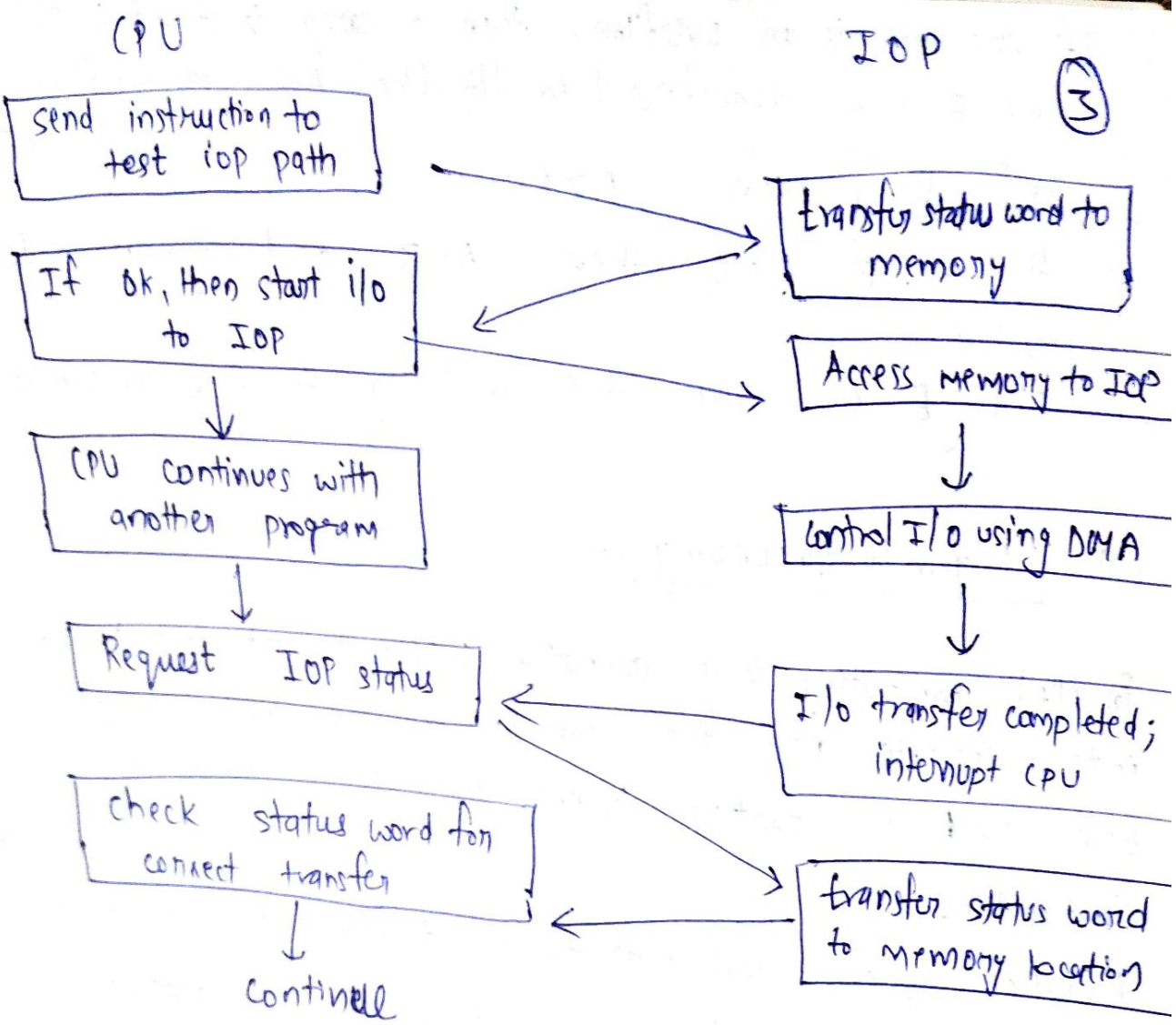
(2)

Ans-(2) Communication channel b/w CPU & IOP:-

There is a comm^n channel b/w CPU & IOP to perform task which come under computer architecture. This channel explains commands executed by IOP & CPU while performing dome programs. The CPU don't executes the instructions but it assigns the task of initiating operations.

→ This channel starts by CPU, by giving "test IOP path" instruction to IOP & then the comm^n begins.

→ Whenever CPU gets interrupt from IOP to access memory, it sends test path instruction to IOP. IOP executes & check for status, if status given to CPU is OK, then CPU gives Start instruction to IOP.



Section (2)

(b)

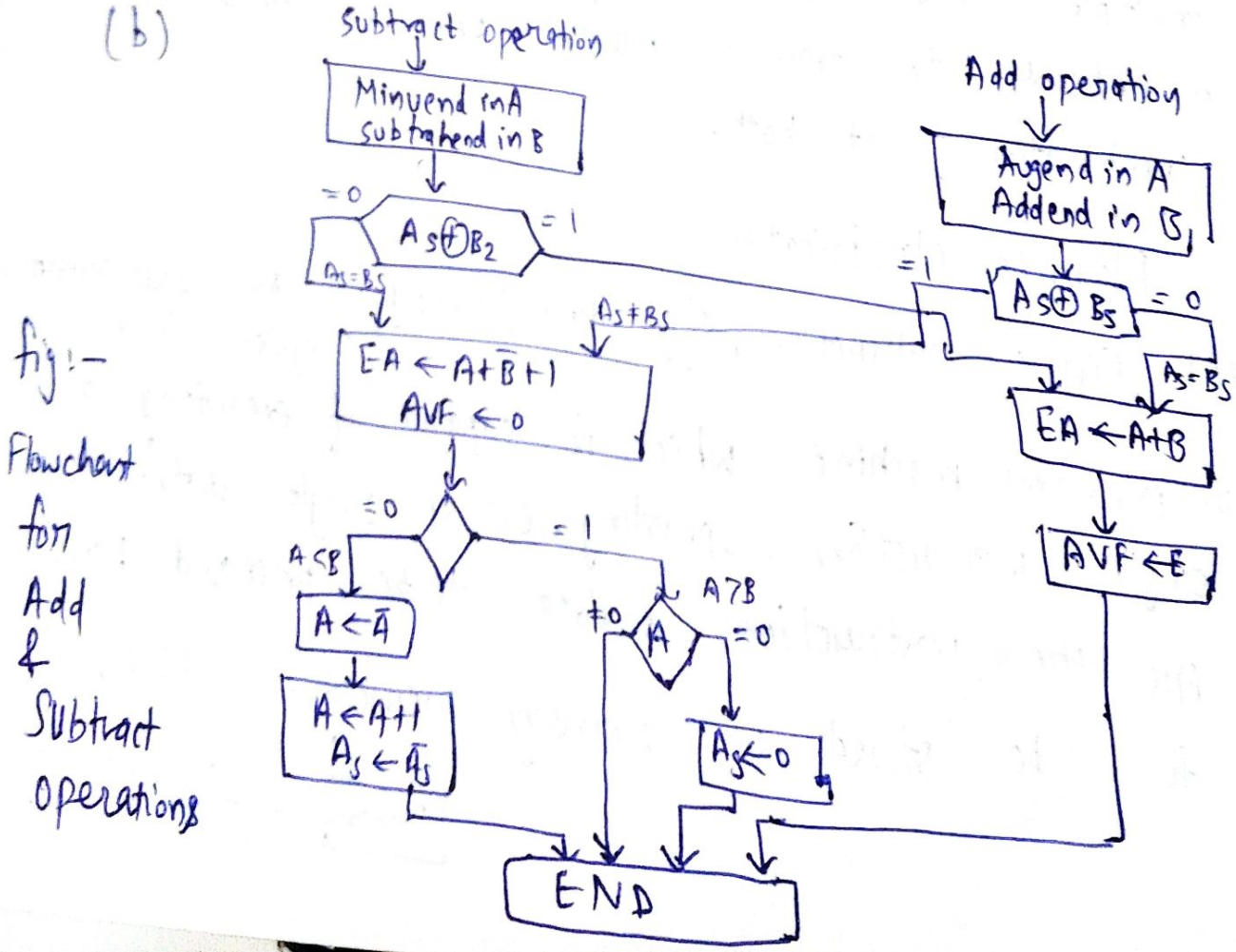


fig:- Flowchart for Add & Subtract operations

If the sum is an overflow, then a carry is stored in E. where E=1 & transferred to flip-flop AVF, add-overflow.

→ If E=1 then A>B (4)

However, if A=0 then A=B and sign is made positive.

→ If E=0 then A<B and sign for A is complemented.

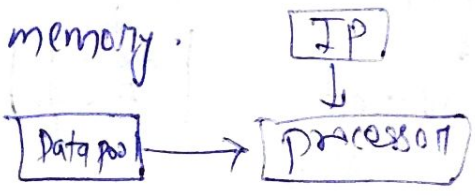
[9] Flynn's taxonomy :-

Parallel computing is a computing where the jobs are broken into discrete parts that can be executed concurrently. Each part is further broken down to a series of instructions.

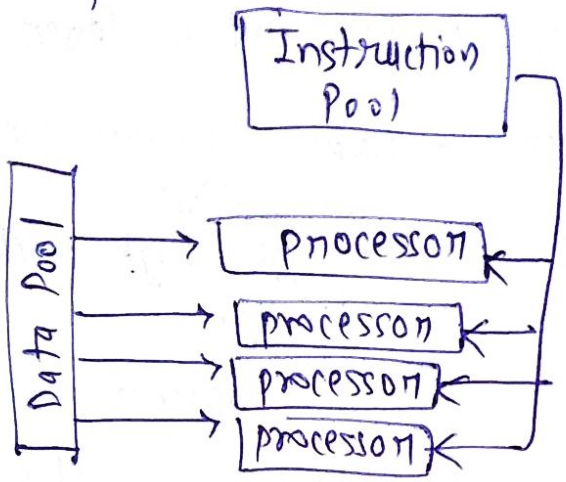
Parallel systems deal with the simultaneous use of multiple computer resources that can include a single computer with multiple processors, a no. of computers connected by a network to form a parallel processing cluster for a combination of both.

Flynn's classification –

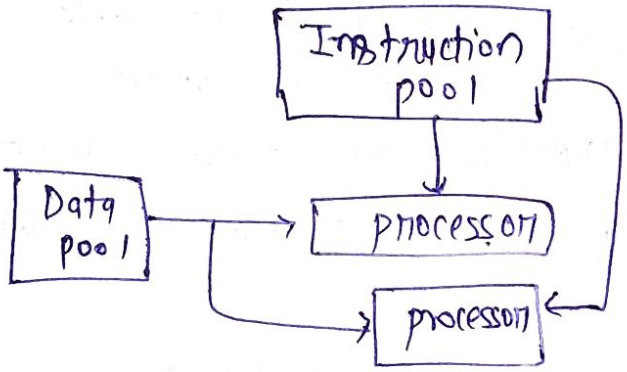
(i) Single-instruction, single-data [SISD] :- An SISD computing system is a uniprocessor machine which is capable of executing a single instruction, operating on a single data-stream. All the instructions & data to be processed have to be stored in primary memory.



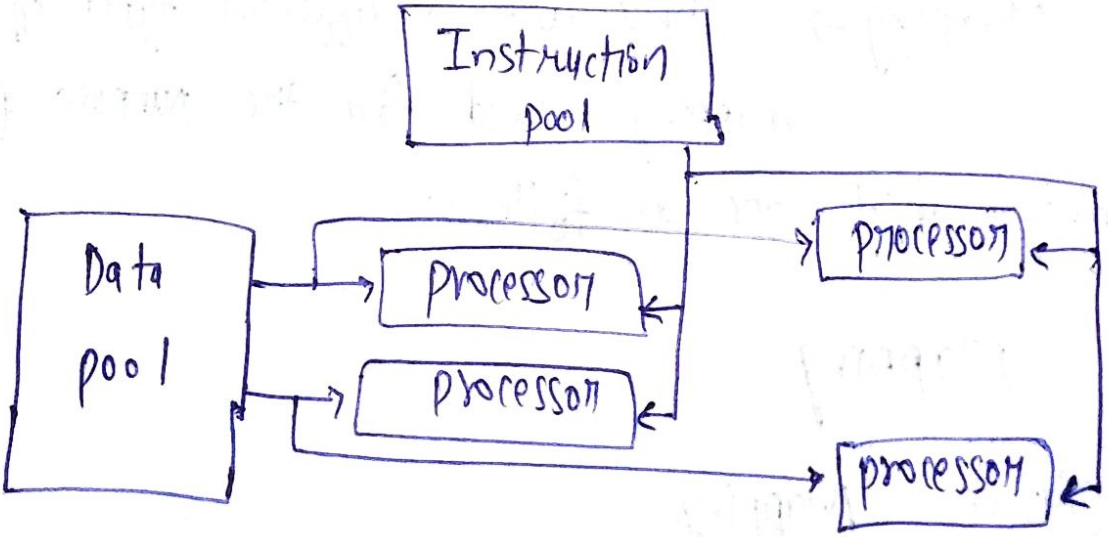
(ii) SIMD :- An SIMD system is microprocessor machine capable of executing the same instruction on all the CPUs but operating on different data streams.



(iii) MISD (Multiple instruction, single-data).



(iv) MIMD :- [Multiple instruction, multiple data]



(f)

SRAM	DRAM
→ It has lower access time, which is faster than DRAM.	→ It is slower than SRAM
→ It is costlier than DRAM.	→ Its cost is lesser to SRAM
→ It consumes more power.	→ DRAM requires reduced power consumptions.
→ It offers low packaging density.	→ It offers high packaging density.
→ Uses transistors & latches.	→ Uses capacitors & transistors
→ SRAM is in the form of on-chip memory.	→ DRAM has characteristics of off-chip memory.
→ It is of smaller size	→ It is available in larger storage capacity.
→ The Storage capacity of SRAM is 1MB to 16MB.	→ The storage capacity of DRAM is 1GB to 16GB.

(e) Cache Memory in Computer Organization

Cache Mapping ⇒ There are 3 different types of mapping used for the purpose of cache memory which are as follows:-

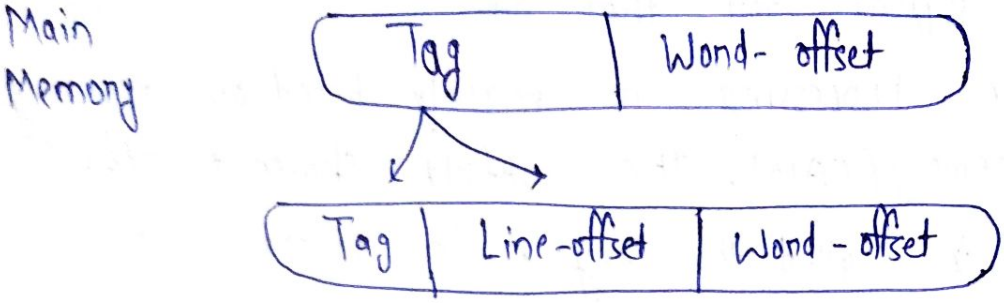
1.) Direct Mapping

2.) Associative Mapping

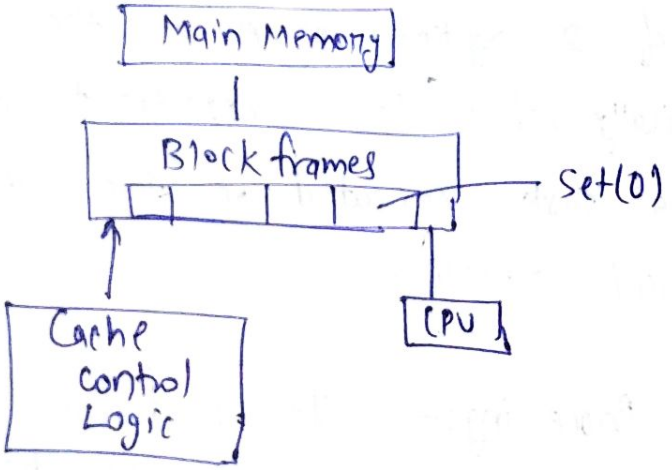
3.) Set-Associative Mapping

(i) Direct Mapping:- It maps each block of main memory into only one possible cache line.

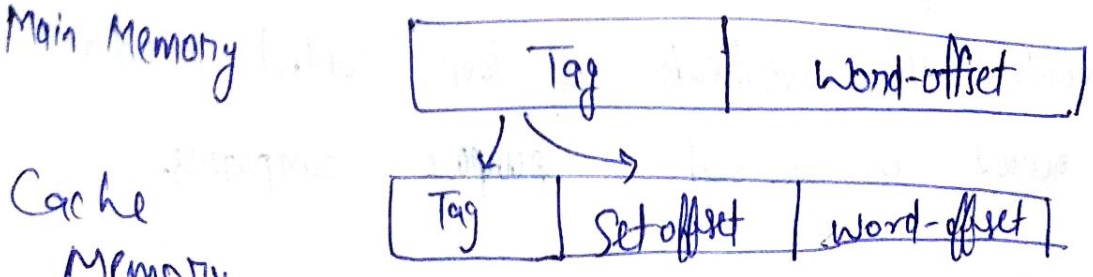
In direct Mapping, assigne each memory block to a specific line in the cache.



(ii) Associative Mapping:- It is used to store content & address of memory word. Any block can go into any line of the cache.



(iii) Set- associative Mapping:- This form of mapping is an enhanced form of direct mapping where drawbacks of direct mapping are removed.



Section - (1)

(a) If a bit in the key register is 1, then corresponding bit in argument & each memory word must be the same to be considered a match ... if a bit in key register is 0, then corresponding bit is considered and memory word are equal for that bit. (8)

→ Associative Processing is mainly based on searching associative Memory (CAM). The subfield chosen to address the memory is called the key. In contrast, for accessing RAM, the physical address of the memory cell is used.

(b) Speedup :- In computer architecture, speedup is a no. that measures the relative performance of 2 systems processing the same problem. More technically, it is the improvement in speed of execution of a task executed on two similar architecture with different resources.

(c) Vector Processing :- It performs the arithmetic operation on the large array of integers or floating-point no. Vector processing operates on all the elements of the array in parallel providing each pass is independent of the other. It avoids the overheads of loop control mechanism that occurs in general purpose computers.

(d) An Input-output processor (IOP) is a processor with direct memory access capability. The IOP provides a path for transfer of data b/w peripherals and memory. (3)

The CPU assigns the task of initiating the i/o program. The IOP operates independent from CPU & transfer data b/w peripherals & memory.

(e) Programmed I/O:- In this mode the data transfer is initiated by the instructions written in a computer program.

Interrupt Initialied I/O:-

This mode uses an interrupt facility and special commands to inform the interface to issue the interrupt command when data becomes available & interface is ready for data transfer.

Er Sahil Ka Gyan